single constraint equation involving an algebraic sum of all the current variables that appear at the node. These constraint equations are algebraic in form.

2.1 Kirchhoff's Voltage Law (KVL)

Consider a dc circuit with many loops as shown in Fig. 2.1-1. Six two-terminal elements are interconnected in this 4-node circuit. The interconnection results in 7 loops in the circuit. The loops are 1-4-2, 2-5-3, 4-6-5, 1-6-3, 1-4-5-3, 2-4-6-3 and 1-6-5-2. The elements are numbered and encircled numbers label the nodes.

Two nodes connected by a piece of connecting wire are equivalent to a single node.

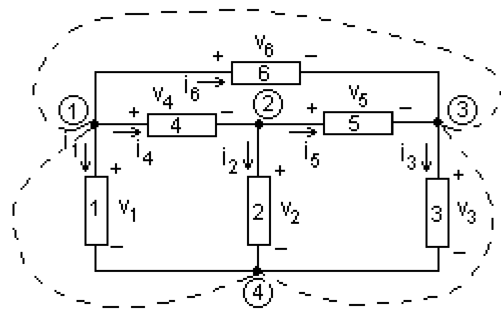

Fig. 2.1-1 A dc circuit with 6-elements, 4-nodes, 7-loops

The circuit is assumed to be in dc steady-state. That is, all the sources in the circuit are assumed to be constant values and all the circuit variables are assumed to be constants in time.

Thus, there is a steady charge distribution at the terminals and on the surface of each two-terminal element in the circuit. The charge distribution produces electrostatic field everywhere. The electrostatic field generated within an element and in the immediate vicinity of an element is proportional to the charge stored on that element. (This is a standard assumption in lumped parameter circuit theory as pointed out in Chapter 1.) The voltage variables marked in Fig. 2.1-1 are the electrostatic potential differences that exist between the terminals of elements. The connecting wires have zero resistance. In addition, there is no charge distribution on the surface of connecting wire.

Imagine that we are carrying a unit positive test charge from node-4 back to the same node by moving it along the path shown by dotted curve in Fig. 2.1-1 in the counter-clockwise direction. The path of travel touches node-1 and node-3. Electrostatic field is a conservative field. Only electrostatic field is present at points lying on the path of travel of unit positive test charge. Therefore, the work to be done in moving the unit positive test charge around this closed path must be zero. v_1 joules is the work to be done in moving a unit positive test charge from node-4 to node-1. v_2 joules is the work to be done in moving a unit positive test charge from node-3 to node-1. And, v_3 joules is the work to be done in moving a unit positive test charge from node-4 to node-3. Therefore,
The work to be done in moving a unit positive test charge from node-4 to node-4 by moving in the dotted path in counter-clockwise direction = (The work to be done in moving a unit positive test charge from node-4 to node-1) + (The work to be done in moving a unit positive test charge from node-1 to node-3) + (The work to be done in moving a unit positive test charge from node-3 to node-4) = $v_1 - v_6 - v_3$ Joules. This has to be zero. Therefore, conservative nature of electrostatic field leads to the following equation involving the three voltage variables appearing in the loop formed by element-1, element-6 and element-3.

$$v_1 - v_6 - v_3 = 0 \tag{2.1-1}$$

If we had taken a unit positive test charge around the same path in clockwise direction, we would have obtained the following equation.

$$v_3 + v_6 - v_1 = 0 \tag{2.1-2}$$

Obviously, Eqn. 2.1-2 must be Eqn. 2.1-1 multiplied by –1. Thus, the direction of traverse of the loop does not matter when we prepare the equation involving voltage variables appearing in that loop.

Now we dispense with the dotted path altogether. Instead, we traverse the loop formed by element-1, element-6 and element-3 in the counter-clockwise direction, starting from node-4. We collect the *voltage rise amounts across each element* as we go along enter these quantities into a sum. Obviously, in this process we are calculating the total work to be done in carrying a unit positive test charge through a path outside the elements, but touching the nodes. Therefore this sum must be zero. The *voltage rise* across the element-1 in the direction of traverse (counter-clockwise direction) is v_1. The *voltage rise* across the element-6 in the direction of traverse is $-v_6$. The *voltage rise* across the element-3 in the direction of traverse is $-v_3$. Therefore, the sum of voltage rises encountered in traversing the loop formed by element-1, element-6 and element-3 in the counter-clockwise direction is $v_1 - v_6 - v_3$. We have already verified that this sum must be equal to zero due to conservative nature of electrostatic field.

If we collect the *voltage drop amounts across each element* as we traverse the loop in counter-clockwise direction and enter them in a sum, we get, $-v_1 + v_6 + v_3$. This sum is equal to zero since this is the work to be done in taking a unit positive test charge around the dotted path in clockwise direction.

Similarly, we could have traversed the loop in clockwise direction and collected the *voltage rises*. The sum of *voltage rises* encountered will be $v_3 + v_6 - v_1$ and will be equal to zero. If *voltage drops* are collected instead, the sum of *voltage drops* will be $-v_3 - v_6 + v_1$ and will be equal to zero.

Or, we could have entered the element voltages that we encounter when we traverse the loop in *counter-clockwise* direction in a sum, with the sign for a particular element voltage variable same as the *polarity of the variable that we meet first when we reach that element.* $-v_1 + v_6 + v_3$ is the result and that is equal to zero. The sum that is formed in this case is called the *algebraic sum of voltages*.

Or else, we could have formed the *algebraic sum of voltages* encountered when we traverse the loop in *clockwise* direction. $v_3 + v_6 - v_1$ is the result and that is equal to zero.

Hence, the constraint appearing among voltage variables of elements in a loop can be obtained by:

(i) traversing the loop in *clockwise* direction and equating the sum of *voltage rises* encountered to zero or

(ii) traversing the loop in *clockwise* direction and equating the sum of *voltage drops* encountered to zero or

(iii) traversing the loop in *counter-clockwise* direction and equating the sum of *voltage rises* encountered to zero or

(iv) traversing the loop in *counter-clockwise* direction and equating the sum of *voltage drops* encountered to zero or

(v) traversing the loop in *clockwise* direction and equating the *algebraic sum of voltages* encountered to zero or

(vi) traversing the loop in *counter-clockwise* direction and equating the *algebraic sum of voltages* encountered to zero.

Different equivalent methods for obtaining the voltage constraint equation for a closed path in a circuit

All the six methods will lead to the same constraint equation. However, in the interest of systematic formulation of circuit equations, it is imperative that we adhere to any one method consistently. We choose the last method in this textbook. <u>Hence, in this textbook, voltage constraint equations are written by traversing the loop in *counter-clockwise* direction and equating the *algebraic sum of voltages* encountered to zero.</u>

The method used in this book for writing voltage constraint equations.

There was nothing special about the particular loop that was chosen to demonstrate the implications arising out of conservative nature of electrostatic field as far as voltage variables in a circuit are concerned. Hence, the same line of reasoning is applicable to all loops in the circuit. Therefore, at least for a dc circuit under steady-state, we can generalise the conclusions we observed above into the following law.

'*The algebraic sum of voltages in any closed path in a circuit is zero.*' *This is called Kirchhoff's Voltage Law.*

Will this law hold good for circuits with time-varying voltage variables too? Consider the same circuit with time-varying voltage variables now as in Fig. 2.1-2.

Lumped parameter circuit theory assumes that induced electric field component caused by time-varying currents in the circuit is negligible everywhere in the space surrounding the devices. Thus, the only force field that is present in the space outside circuit elements is the field generated by the coulomb force (that is, the force that depends only on charges and the distance between charges as per inverse square law) arising out of charge distributions on the circuit elements. The quantity of charge stored in each element in a circuit will change with time in a circuit containing time-varying sources. Therefore, the force field in the space outside the elements too will vary with time. However, at any instant *t*, the force field is dependent only on the charges stored in elements at that instant and the spatial distances involved. The term 'electrostatic field' does not imply that the value and direction of this field are constant in time. Rather, it means that the field arises out of 'coulomb force term'. Thus, we can use the term 'electrostatic field' to represent the force field arising out of 'coulomb force terms' even when the charge distributions on the elements vary with time.

The conservative nature of a force field arising out of 'coulomb force' is a direct result of inverse square dependence on distances displayed by such forces. Such a force field remains a 'conservative field' even if it is varying with time.

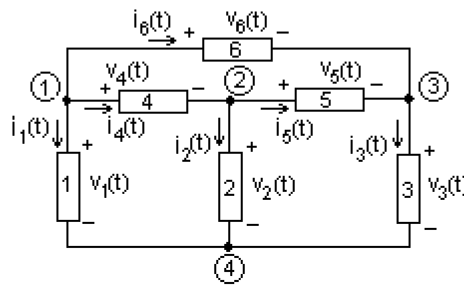

Fig. 2.1-2 A 4-node, 6-element, 7-loop circuit with time-varying voltages and currents

The conservative nature of a force field arising out of 'coulomb force' is a direct result of inverse square dependence on distances displayed by such forces. Therefore, if only coulomb force field is present in the space surrounding a circuit, the work integral – [*i.e.*, $-\oint \vec{E}_S \cdot \vec{dl}$ where $\vec{E}_S$ is the 'coulomb force field' or electrostatic field], evaluated at any instant *t* over any closed path lying outside the circuit elements, will be zero quite irrespective of whether the 'coulomb force field' is time-varying or not. Therefore, the algebraic sum of instantaneous value of voltage variables in any loop in the circuit must be zero.

However, we have been accustomed to interpret the work integral $-\oint \vec{E}_S \cdot \vec{dl}$ as the work to be done in carrying a unit positive test charge around a closed path in the $\vec{E}_S$ field quasi-statically. We face a problem in carrying over this interpretation to a time-varying situation. We have to move this unit test charge slowly around the loop. But then, the work we calculate will be the work done against $\vec{E}_S$ at different instants at different locations since we can't be moving that test charge with infinite speed in the closed path. That is not the same as the value of integral $-\oint \vec{E}_S \cdot \vec{dl}$ at a particular time instant *t*.

However, the only field that is present in the space around elements in a time-varying circuit is the electrostatic field. Therefore, the field outside the elements at any instant *t* will be the same as the *electrostatic field* that would exist in a *dc circuit* with same elements and same geometry, but with all charge variables, voltage variables and current variables in the circuit frozen at the values they had at the time instant *t*. Imagine that we are carrying a unit positive test charge around a closed loop in this *frozen circuit*. The work to be done in this process will be zero since the charge was taken around a closed path in a *steady conservative field*. Therefore, the algebraic sum of voltage variables in any loop in this *frozen circuit* must be zero. But, that will imply that, the algebraic sum of instantaneous value of voltage variables, at any *t*, in any loop in the circuit with time-varying voltages, must be equal to zero.

Therefore, KVL is valid under time-varying conditions too. The complete statement of KVL follows.

Statement of Kirchhoff's Voltage Law for a lumped parameter circuit.

Kirchhoff's Voltage Law states that the algebraic sum of voltages in any closed path in a lumped parameter circuit is zero on an instant to instant basis.

It may alternatively be stated in terms of *voltage rises* or *voltage drops* as below.

Alternative statements for Kirchhoff's Voltage Law

Kirchhoff's Voltage Law states that the sum of 'voltage rises' in any closed path in a lumped parameter circuit is zero on an instant to instant basis.

Kirchhoff's Voltage Law states that the sum of 'voltage drops' in any closed path in a lumped parameter circuit is zero on an instant to instant basis.

The circuit in Fig. 2.1-2 has 7 loops. The loops are 1-4-2, 2-5-3, 4-6-5, 1-6-3, 1-4-5-3, 2-4-6-3 and 1-6-5-2 where the numbers refer to the element labels.

The KVL equations for these loops are derived below.

$$\begin{aligned}
&\text{Loop } 1-4-2 &&: -v_1(t)+v_4(t)+v_2(t)=0\\
&\text{Loop } 2-5-3 &&: -v_2(t)+v_5(t)+v_3(t)=0\\
&\text{Loop } 4-6-5 &&: -v_4(t)+v_6(t)-v_5(t)=0\\
&\text{Loop } 1-6-3 &&: -v_1(t)+v_6(t)+v_3(t)=0\\
&\text{Loop } 1-4-5\text{-}3 &&: -v_1(t)+v_4(t)+v_5(t)+v_3(t)=0\\
&\text{Loop } 2-4-6\text{-}3 &&: -v_2(t)-v_4(t)+v_6(t)+v_3(t)=0\\
&\text{Loop } 1-6-5\text{-}2 &&: -v_1(t)+v_6(t)-v_5(t)+v_2(t)=0
\end{aligned}$$

We observe that the first three equations will form an independent set of three equations. But the fifth equation can be obtained by adding the first two equations together. When Loop 1-4-2 equation is added to Loop 2-5-3 equation, the term $v_2(t)$ appears twice with opposite signs. Thus the resulting equation must be that of a loop formed by 1-4-5-3. Similarly, Loop 2-5-3 equation added to Loop 4-6-5 equation should result in Loop 2-4-6-3 equation. Sum of the first three equations must be same as the fourth equation.

Some KVL equations can be obtained by adding other KVL equations together.

Thus not all the 7 equations are independent. In fact, in a non-degenerate circuit containing *b*- elements, *n*-nodes and *l*-loops there will be exactly (*b*-*n*+1) loop equations that are independent. *l* will be more than or equal to (*b*-*n*+1). We will prove these statements in the last chapter on Network Topology in this book. We accept these statements without proof at this point.

The set of all loop equations in a circuit will not be an independent set of equations.

This does not mean that a random selection of (*b*-*n*+1) loop equations from the set of *l* loop equations will be an independent set of loop equations. For instance, in the present example, there must be (6-4+1) = 3 independent loop equations. However, the loop equations for Loop 1-4-2, Loop 2-5-3 and Loop 1-4-5-3 are not independent. The third can be obtained by adding first two. Note that the first two loops are completely contained by the third loop. A *planar circuit* is one that can be drawn on paper without any crossing of connection wires. A *basic window* in a *planar circuit* is a loop that does not contain any other loop within it. It must be intuitively clear that the loop equations for the *basic windows* of the *planar circuit* will form an independent set of loop equations. These *basic windows* of a *planar circuit* are called its '*meshes*'.

An arbitrary set of loop equations may not form an independent set of equations.

Example : 2.1-1

The source voltages of four independent voltage sources in the circuit in Fig. 2.1-3 are given as v_{S1}=10 volts, v_{S2} = 10sin100*t* volts, v_{S3} = 10cos100*t* volts and v_{S4} = 10 volts. v_3 is observed to have a zero average value. The time-varying component of v_1 is seen to be 10sin(100*t*-30^0) volts. Find v_1, v_2 and v_3 as functions of time.

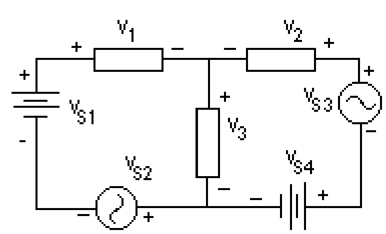

Fig. 2.1-3 Circuit for Example : 2.1-1

Solution

v_3 is stated to have a zero average. This implies that v_3 has a zero dc content. Thus v_3 can be written as $v_3 = A\sin(100t - \theta)$ volts where A and θ are to be found. v_1 is stated to have a time-varying component of 10sin(100*t*-30^0) volts. It may have a dc content too. Thus, $v_1 = B + 10\sin(100t-30^0)$ volts where B is to be found. v_2 may contain both dc and time-varying components. Thus, $v_2 = C + D\sin(100t - \phi)$ volts where C, D and ϕ have to be found.

Apply KVL in the first loop. The KVL equation is:

$$-v_{s1}+v_1+v_3+v_{s2}=0$$

$$i.e.,\ -10+(B+10\sin(100t-30^0))+A\sin(100t-\theta)+10\sin 100t=0$$

This equation involves some constants and some sinusoidal functions. This equation is the result of applying KVL to a loop in a circuit. Therefore, this equation has to be true at all t. Therefore, the equation can be split into two equations that have to be satisfied simultaneously. This is so since a constant can not be balanced by a sinusoidal function in an equation for all t.

$$-10+B=0 \ \text{ and } \ 10\sin(100t-30^0)+A\sin(100t-\theta)+10\sin 100t=0$$

First equation yields B = 10 volts. Second equation is simplified by employing trigonometric identities as below.

$$5\sqrt{3}\sin 100t-5\cos 100t+(A\cos\theta)\sin 100t-(A\sin\theta)\cos 100t+10\sin 100t=0$$

This equation can be true for all t only if the coefficient of sin100t is zero and the coefficient of cos100t is zero independently.

$$\therefore 5\sqrt{3}+A\cos\theta+10=0 \ \text{ and } \ -5-A\sin\theta=0$$

$$\therefore A\cos\theta=-10-5\sqrt{3}=-18.66\ ;\ A\sin\theta=-5$$

$$\therefore A=19.32 \ \text{ and } \ \theta=\tan^{-1}\frac{-5}{-18.66}=180+\tan^{-1}\frac{5}{18.66}=195^0$$

$$\therefore v_1=10+10\sin(100t-30^0)\ \text{volts and}\ v_3=19.32\sin(100t-195^0)\ \text{volts.}$$

Now apply KVL in the outer loop to get,

$$-v_{s1}+v_1-v_2+v_{s3}+v_{s4}+v_{s2}=0$$

$$i.e.,\ -10+(10+10\sin(100t-30^0))-C-D\sin(100t-\phi)+10\cos(100t)$$
$$+10+10\sin 100t=0$$

$$(10+10\sin(100t-30^0))-C-D\sin(100t-\phi)+10\cos(100t)+10\sin 100t=0$$

$$\therefore C=10 \ \text{ and}$$

$$10\sin(100t-30^0)-D\sin(100t-\phi)+10\cos 100t+10\sin 100t=0$$

$$8.66\sin 100t-5\cos 100t-(D\cos\phi)\sin 100t+$$
$$(D\sin\phi)\cos 100t+10\cos 100t+10\sin 100t=0$$

$$\therefore D\cos\phi=18.66\ ;\ D\sin\phi=-5 \Rightarrow D=19.32 \ \text{ and } \ \phi=\tan^{-1}\frac{-5}{18.66}=-15^0$$

$$\therefore v_2=10+19.32\sin(100t+15^0)\ \text{volts.}$$

Therefore, $v_1=10+10\sin(100t-30^0)$ volts, $v_2=10+19.32\sin(100t+15^0)$ volts and $v_3=19.32\sin(100t-195^0)$ volts is the required answer.

The key to the solution of this problem is the point that KVL has to be satisfied at all time instants.

Example : 2.1-2

Express the terminal voltages of elements 2, 3 and 5 in terms of terminal voltages of elements 1, 4 and 6 in the circuit in Fig. 2.1-4.

Solution

Applying KVL in the loop 1-4-2, we get, $-v_1(t)+v_4(t)+v_2(t)=0$.

$$\therefore v_2(t)=v_1(t)-v_4(t)$$

Applying KVL in the loop 4-5-6, we get, $v_4(t)+v_5(t)-v_6(t)=0$.

$$\therefore v_5(t)=v_6(t)-v_4(t)$$

Applying KVL in the loop 1-6-3, we get, $-v_1(t)+v_6(t)+v_3(t)=0$.

$$\therefore v_3(t)=v_1(t)-v_6(t)$$

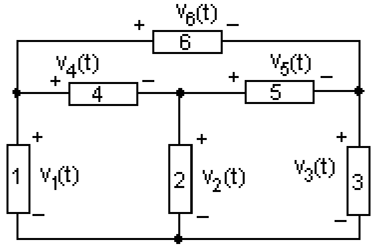

Fig. 2.1-4 Circuit for Example : 2.1-2

2.2 Kirchhoff's Current Law

Conservation law of charge states that charges can neither be created or destroyed in a given volume. Hence, if more positive charge flows into a volume at any instant *t* than the positive charge that flows out of the volume at the same instant, then, the net charge stored inside the volume must be increasing at that instant. Similarly, if more positive charge flows out of the volume than what flows into the volume at that instant, then, the net charge stored within must be decreasing at that instant. Therefore, the *net positive current* that flows into the volume at an instant *t* must be equal to the *rate of change* of *net charge* stored within that volume at that instant. A mathematical statement of this fact is called the *continuity equation for currents*.

Continuity equation for currents

If, for some reason or other, the net charge inside the volume is either constrained to remain at zero at all instants or is constrained to remain at some constant value at all instants, then, the *net positive current* that flows into the volume must be zero at all instants.

Lumped parameter circuit theory assumes that the surface charge distribution on the surface of connecting wires is negligible at all instants of time. There is surface charge distribution on all circuit elements other than the connecting wires. In general, these surface charge distributions are time-varying too. However, the positive charge and negative charge distributed on the surface of any two-terminal element or four-terminal element are equal in magnitude at all time instants under quasi-static conditions. Therefore, if we consider a volume that contains some circuit elements completely within, those elements will contribute only zero net charge to the net charge storage within the volume. The situation would, however, be different if the volume intersects some element. For instance, consider a volume that encloses only one of the plates of a capacitor. Then, there will be net charge storage within the volume and that may change with time too.

Therefore, we restrict ourselves to a volume that intersects connecting wires at many places without enclosing or intersecting even single circuit element or a volume that intersects connecting wires at many places and completely encloses one or more circuit elements. We do not permit the volume to intersect any circuit element.

Since an element completely enclosed within a volume does not contribute to net charge within the volume and since the connecting wires have only negligible surface charge distributions on them, it follows that, the net charge contained in a volume chosen the way suggested in the previous paragraph will be zero at all *t*. Therefore, the rate of change of net charge will also be zero at all *t*. *Then, by continuity equation for currents, the net positive current that flows into the volume through the wires must be zero at all time-instants.*

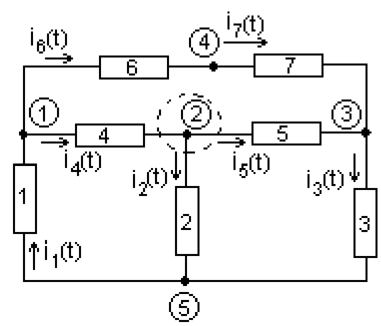

Fig. 2.2-1 Circuit for illustrating Kirchhoff's Current Law

A *node* in a circuit is part of connecting wire. Therefore, there is no charge storage at a *node* in a circuit as per the assumptions employed by lumped parameter circuit theory. Therefore, there is no rate of change of charge storage too. Consider a special volume – a volume that encloses a node in a circuit and intersects all the wires connected at that node. Then, the reasoning outlined above leads us to the conclusion that the *net positive current* that flows into the volume through all the connecting wires that were intersected by the volume (*i.e.,* all the wires connected together at that node) should be zero at all *t*. Equivalently, we may state that, *net positive current* that flows out of the volume must be zero at all *t*.

Consider a volume denoted by the dotted circle around node-2 in the circuit in Fig. 2.2-1. This volume intersects three wires, encloses the node-2 and does not enclose any circuit element. Neither does it intersect any circuit element other than the connecting wires. Therefore, the *net positive current flowing out of the volume* must be zero. This fact leads to the following equation.

$$-i_4(t)+i_2(t)+i_5(t)=0 \qquad (2.2\text{-}1)$$

$i_4(t)$ is a current that flows *into* the volume. We need a minus sign to make it a current that flows *out of* the volume. Hence the minus sign in front of $i_4(t)$ in the Eqn. 2.2-1.

We could have arrived at an equation containing the same information contained in Eqn. 2.2-1 by stipulating that *net positive current flowing into the volume* must be equal to zero. The equation that results will be:

$$i_4(t) - i_2(t) - i_5(t) = 0 \qquad (2.2\text{-}2)$$

Eqn. 2.2-2 is, obviously, Eqn. 2.2-1 multiplied by –1 and contains the same information.

We could have arrived at Eqn. 2.2-1 by stipulating that the *algebraic sum* of currents *leaving* a node must be equal to zero. '*Algebraic sum*' in this case implies that if a particular current variable has its *reference direction* pointing *towards* the node, it has to enter the equation with *negative* sign. If a particular current variable has its *reference direction* pointing *away* from node it has to be entered in the equation with *positive* sign.

Similarly, we could have arrived at Eqn. 2.2-2 by stipulating that the *algebraic sum* of currents *entering* a node must be equal to zero. '*Algebraic sum*' in this case implies that if a particular current variable has its *reference direction* pointing *towards* the node, it has to enter the equation with a *positive* sign. If a particular current variable has its *reference direction* pointing *away* from node it has to be entered in the equation with *negative* sign.

Obviously, all the four methods of arriving at the node equation are equivalent. However, in the interest of a systematic procedure, we use the stipulation that the *algebraic sum* of currents *leaving* a node must be equal to zero. We are ready to state the Kirchhoff's current law now.

Statement of Kirchhoff's Current Law

Kirchhoff's Current Law (KVL) states that the algebraic sum of currents leaving a node in a lumped parameter circuit is equal to zero on an instant to instant basis.

KCL at a node can be stated in alternative ways.

Alternative forms of KCL

Kirchhoff's Current Law (KVL) states that the algebraic sum of currents entering a node in a lumped parameter circuit is equal to zero on an instant to instant basis.

Kirchhoff's Current Law (KVL) states that the sum of currents entering a node in a lumped parameter circuit through some wires must be equal to the sum of currents leaving the same node through the remaining wires on an instant to instant basis.

KCL equations at all nodes of the circuit shown in Fig. 2.2-1 are derived below.

$$\begin{aligned}
\text{Node}-1: &\ -i_1(t) + i_4(t) + i_6(t) = 0\\
\text{Node}-2: &\ -i_4(t) + i_2(t) + i_5(t) = 0\\
\text{Node}-3: &\ \quad i_3(t) - i_5(t) - i_7(t) = 0\\
\text{Node}-4: &\ -i_6(t) + i_7(t) \qquad\quad = 0\\
\text{Node}-5: &\ \quad i_1(t) - i_2(t) - i_3(t) = 0
\end{aligned}$$

Note that the sum of these equations will be of $0 = 0$ form. This indicates that these five equations do not form an independent set of equations. If we add all KCL equations derived for all the nodes of a circuit, a particular current variable that enters some equation with positive sign will necessarily enter some other equation in the set with a negative sign. After all, an element has to get connected to two nodes. Therefore, all terms in the left-hand side of the sum will get cancelled. Suppose we discard the KCL equation at any one node. At least two elements must be connected to any node. Therefore, the sum of four of the five KCL equations will have at least two current variables present in the left-hand side. Therefore, any set of four KCL equations will be an independent set of equations. *Thus, in general, there will be (n-1) independent KCL equations in an n-node circuit.*

There will be (n-1) independent KCL equations at nodes in an n – node lumped parameter circuit.

We had earlier accepted the fact that there will be (b – n +1) independent KVL equations for a b-element, n-node, l-loop lumped parameter circuit. (b – n +1) independent KVL equations together with (n-1) independent KCL equations make the required b interconnection equations needed to solve the circuit.

It is possible to arrive at a more general form of KCL applicable to lumped parameter circuits by considering a closed surface that encloses more than one node along with one or more elements. We have reasoned earlier in this section that the net charge contained inside such a closed surface must be equal to zero. Therefore, the algebraic sum of currents leaving such a closed surface must be equal to zero on an instant to instant basis. Such a closed surface will contain two or more nodes and all the elements that are connected between the nodes that are within the closed surface. Such a closed surface is called a *supernode*.

'Supernode' defined

How many nodes can a circuit with n nodes have? Taking two at a time there are ${}^{n}C_2$ supernodes that contain two nodes each. Similarly there are ${}^{n}C_3$ supernodes that contain three nodes each. See the circuit in Fig. 2.2-2.

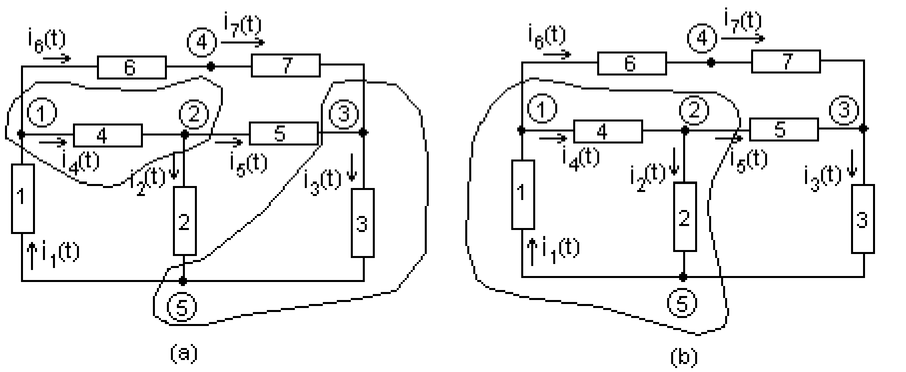

Fig. 2.2-2 (a) Circuit showing two supernodes with two nodes each (b) Circuit showing a supernode that contains three nodes

Two supernodes, each containing two nodes, are shown in the circuit in (a) of Fig. 2.2-2. One supernode containing three nodes is shown in the circuit in (b) of Fig. 2.2-2.

Kirchhoff's Current Law is applicable to supernodes too.

Therefore, the KCL equation for the supernode containing node-1 and node-2 is obtained as $-i_1(t)+i_6(t)+i_2(t)+i_5(t)=0$. Obviously, this must be the sum of KCL equations written for node-1 and node-2. Similarly, the KCL equation for the supernode in the circuit (b) in Fig. 2.2-2 must be the sum of KCL equations written for node-1, node-2 and node-5. This may be verified.

KCL for a supernode can be obtained by adding the KCL equations for all the nodes that are included within the supernode.

The total number of KCL equations that can be written for an n –node circuit is equal to ${}^{n}C_1+{}^{n}C_2+{}^{n}C_3+........+{}^{n}C_{n-1}$. This series has a sum equal to 2^n-2 .

Only (n-1) independent equations from these 2^n-2 KCL equations can be used for solving the circuit.

Example : 2.2-1

Find the power delivered by all the sources in the circuit in Fig. 2.2-3.

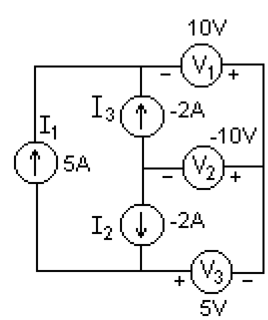

Fig. 2.2-3 Circuit for Example : 2.2-1

Solution

Currents through the voltage sources and voltage across the current sources have to be obtained first. The circuit with all nodes and reference directions for variables identified is shown in Fig. 2.2-4.

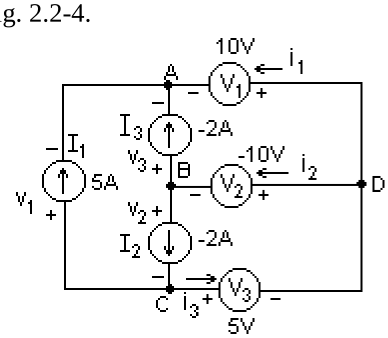

Fig. 2.2-4 Circuit in with nodes and reference directions identified

Applying KCL at node-A, we get, –5– (–2) –i_1 = 0 ⇒ i_1 = –3A

Applying KCL at node-B, we get, (–2) + (–2) – i_2 = 0 ⇒ i_2 = – 4A

Applying KCL at node-C, we get, 5 – (–2) + i_3 = 0 ⇒ i_3 = –7A

Applying KVL in the loop I_1-V_1-V_3, we get, v_1 –10–5 = 0 ⇒ v_1 = 15 volts

Applying KVL in the loop I_3-V_1-V_2, we get, v_3 –10+ (–10) = 0 ⇒ v_3 = 20 volts

Applying KVL in the loop I_2-V_2-V_3, we get, –v_2 – (–10) –5 = 0 ⇒ v_2 = 5 volts

Power *delivered by an element* is given by –*vi* where *v* and *i* are its voltage and current variables as per passive sign convention.

∴Power delivered by I_1 source = –v_1 ×5 A= –75 W

Power delivered by I_2 source = –v_2 × (–2) A= 10 W

Power delivered by I_3 source = –v_3 × (–2) A= 40 W

Power delivered by V_1 source = –10V × i_1 = 30 W

Power delivered by V_2 source = –(–10V) × i_2 = – 40 W

Power delivered by V_3 source = –5V × i_3 = 35 W

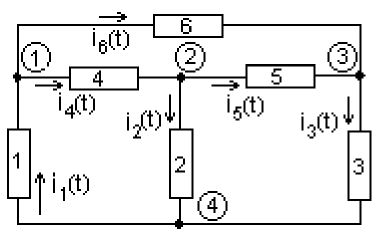

Fig. 2.2-5 Circuit for Example : 2.2-2

Example : 2.2-2

Express $i_2(t)$, $i_4(t)$ and $i_5(t)$ in terms of $i_1(t)$, $i_3(t)$ and $i_6(t)$ in the circuit shown in Fig. 2.2-5.

Solution

Applying KCL at node-1, we get, $-i_1(t)+i_4(t)+i_6(t)=0 \Rightarrow i_4(t)=i_1(t)-i_6(t)$

Applying KCL at node-3, we get, $-i_5(t)+i_3(t)-i_6(t)=0 \Rightarrow i_5(t)=i_3(t)-i_6(t)$

Applying KCL at node-2, we get, $-i_4(t)+i_2(t)+i_5(t)=0 \Rightarrow i_2(t)=i_4(t)-i_5(t) = i_1(t)-i_3(t)$

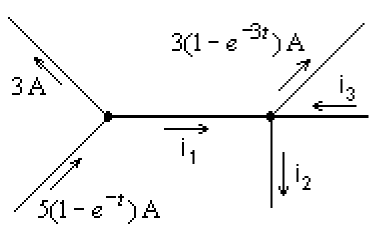

Fig. 2.2-6 Part of a circuit referred to in Example : 2.2-3

Example : 2.2-3

Fig. 2.2-6 shows the connecting wires in a part of a circuit. Some of the currents are specified for $t \geq 0$ in Fig. 2.2-6. The current i_2 is seen to be a constant in time. The current i_3 is seen to approach zero as $t \to \infty$. Find i_1, i_2 and i_3 for $t \geq 0$.

Solution

Applying KVL at first node, we get, $3+i_1-5(1-e^{-t})=0 \Rightarrow i_1=2-5e^{-t}$ A

i_2 is stated to be a constant in time. Let i_2 = *A*. i_3 is stated to approach zero as $t \to \infty$. This implies that there is no dc component in i_3. It may contain both e^{-t} and e^{-3t} components. Let $i_3 = C\,e^{-t} + D\,e^{-3t}$ A. Then, applying KCL at the second node, we get,

$$-i_1+3(1-e^{-3t})-i_3+i_2=0$$
$$i.e.,\ -2+5e^{-t}+3-3e^{-3t}-Ce^{-t}-De^{-3t}+A=0$$
$$i.e.,\ (A+1)+e^{-t}(5-C)+e^{-3t}(-3-D)=0$$

KCL remains true at all *t*. Hence the last equation must be valid for all $t \geq 0$. No time varying function can remain equal to a constant unless that function itself is a constant. Thus, (*A*+1) term in the last equation can not be balanced by e^{-t} and e^{-3t} terms for all $t \geq 0$. Therefore, (*A*+1) has to be zero.

∴*A* = -1 ⇒ i_2 = –1 A.

A term involving e^{-t} can not get balanced by another term that involves e^{-3t} for all $t \geq 0$. Therefore, coefficient of e^{-t} must be zero and coefficient of e^{-3t} too must be zero. Therefore, (5-*C*) = 0 and (3+*D*) = 0.

∴*C* = 5 and *D* = –3 ⇒ $i_3 = (5\,e^{-t} - 3\,e^{-3t})$ A.

The solution is marked in Fig. 2.2-7.

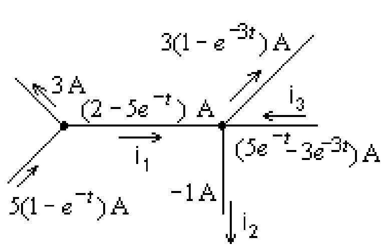

Fig. 2.2-7 Solution for Example : 2.2-3