

Example : 11.2-2

A capacitor C is initially charged to 500 V and is left open for 120 sec. The voltage across capacitor at the end of this time interval is seen to be 400 V. A resistor of 100 k Ω is connected across this capacitor at 120 sec. The voltage across capacitor is found to reach 100 V at 216.4 sec after this connection has been made. Find the value of C and its leakage resistance.

Solution

Let R be the leakage resistance of the capacitor. Then, using Eqn. 11.2-2 with suitable values for V_o and $v_C(t)$,

$$400 = 500 e^{-120/\tau_1} \Rightarrow \tau_1 = \frac{120}{\ln 1.25} = 537.8 \text{ sec}$$

and

$$100 = 400 e^{-216.4/\tau_2} \Rightarrow \tau_2 = \frac{216.4}{\ln 4} = 156.1 \text{ sec}$$

where $\tau_1 = RC$ and $\tau_2 = [R // 100 \text{ k}\Omega]C$

$$\therefore \frac{\tau_1}{\tau_2} = \frac{537.8 \text{ sec}}{156.1 \text{ sec}} = 3.445 = \frac{R(R+100)}{R \times 100} = \frac{(R+100)}{100} = 0.01R + 1; \text{ with } R \text{ in k}\Omega$$

$$\therefore R = 244.5 \text{ k}\Omega \text{ and since } RC = 537.8 \text{ sec, } C = \frac{537.8 \text{ sec}}{244.5 \text{ k}\Omega} = 2.2 \text{ mF} = 2200 \mu\text{F}$$

11.3 Zero-State Response of RC Circuits for Various Inputs

We consider the response of Series RC Circuit and Parallel RC Circuit for various input source functions in this section. We know that the total response of any circuit to application of input function is obtained by adding the zero-input response and zero-state response together. Hence we consider only the zero-state response part for various input source functions in this section. We begin with impulse response (i.e., zero-state impulse response) first.

Impulse Response of First-Order RC Circuits

The Series RC Circuit in (a) of Fig. 11.3-1 has zero initial condition and is excited by a unit impulse voltage source. The capacitor can not absorb the impulse voltage. Hence the resistor absorbs the impulse voltage and as a result an impulse current of $1/R$ coul flows through the circuit. This impulse current flow results in sudden dumping of $1/R$ coulombs of charge on the capacitor plates; thereby changing the capacitor voltage from 0 at $t = 0^-$ to $1/RC$ Volts at $t = 0^+$. The unit impulse voltage source is a short circuit for $t \geq 0^+$. Therefore, the only effect of impulse voltage application is to change the initial condition of the capacitor instantaneously. The circuit effectively becomes a source-free circuit with initial energy for $t \geq 0^+$ and executes its zero-input response. The relevant circuit is shown in (b) of Fig. 11.3-1.

Initial voltage across capacitor is $1/RC$ Volts and all the voltages and currents in the circuit decay exponentially to zero with a time constant of $\tau = RC$ seconds.

$$v_C(t) = -v_R(t) = \frac{1}{RC} e^{-t/\tau} \text{ volts for } t \geq 0^+$$

$$i_C(t) = i_R(t) = \frac{1}{R^2 C} e^{-t/\tau} \text{ amps for } t \geq 0^+$$

We had noticed the equivalence between non-zero initial condition at $t = 0^-$ and application of impulse at $t = 0$ in our analysis of RL Circuits. We see that it is true in the case of RC circuits too. Specifically, a capacitor with an initial voltage of V_o Volts across it at $t = 0^-$ may be replaced by a capacitor with zero initial voltage and a impulse current source of suitable magnitude (CV_o coul) and suitable polarity connected across it. This equivalence is shown in Fig. 11.3-2.

Fig. 11.3-3 shows the application of a unit impulse current to a parallel RC circuit with zero initial energy. The resistor can not support the impulse current. If it were to do so, it would have called for an impulse voltage across it and that will be resisted by the

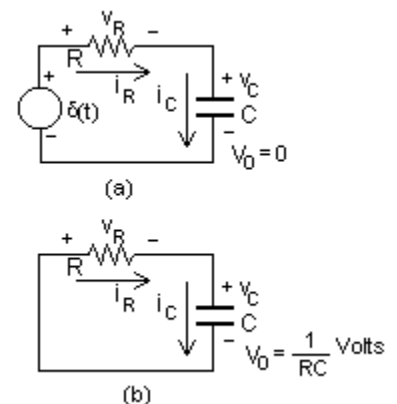


Fig. 11.3-1 Pertaining to Impulse Response of Series RC Circuit

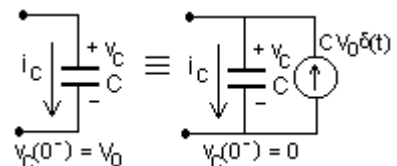


Fig. 11.3-2 Equivalence Between Non-Zero Initial Voltage and Impulse Current Application in RC Circuits

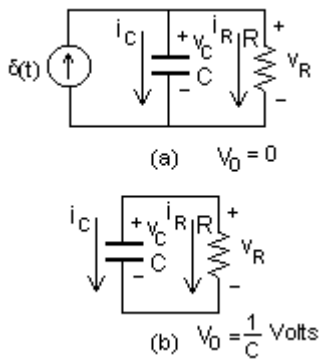


Fig. 11.3-3 Pertaining to Unit Impulse Response of Parallel RC Circuit

capacitor in parallel. Therefore, all the impulse content goes through the capacitor, changing its voltage by $1/C$ Volts instantaneously from 0 at $t = 0^-$ to $1/C$ Volts at $t = 0^+$. The unit impulse current source is effectively an open-circuit after $t = 0^+$. Therefore, the circuit becomes a *source-free* circuit for $t \geq 0^+$ and executes its zero-input response ((b) in Fig. 11.3-3).

Therefore,

$$v_C(t) = v_R(t) = \frac{1}{C} e^{-t/\tau} \text{ volts for } t \geq 0^+$$

$$i_R(t) = -i_C(t) = \frac{1}{RC} e^{-t/\tau} \text{ amps for } t \geq 0^+$$

Example : 11.3-1

The value of I in the circuit in Fig. 11.3-4 is 3×10^{-6} coul. Find the zero-state response for the current through the 10k resistor in the direction marked in the figure.

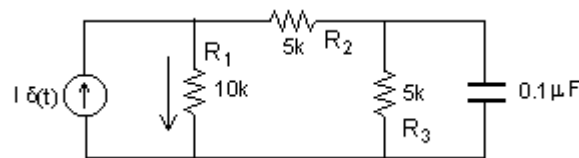


Fig. 11.3-4 Circuit for Example : 11.3-1

Solution

The voltage across the capacitor can, at best, change by a *finite* amount as a result of impulse current flow. This implies that the current through the 5k resistor (R_3) across the capacitor can not be an impulse. Therefore, the capacitor effectively shorts the 5k resistor across it as far as the impulse current flow is concerned. Hence the $3 \times 10^{-6} \delta(t)$ gets shared by 10k and the other 5k (R_2) as per the current division principle in parallel resistors. Thus $2 \times 10^{-6} \delta(t)$ goes through the other 5k resistor (R_2) and the $0.1 \mu F$ capacitor. This results in sudden dumping of $2 \mu C$ of charge across the capacitor, raising its voltage to 20 Volts at $t = 0^+$. The current source goes open for $t \geq 0^+$ and the circuit executes its zero-input response.

Time constant of the circuit can be found by obtaining the equivalent resistance connected across the capacitor. The equivalent resistance is $5k // 15k = 3.75k$. Therefore $\tau = 0.375$ ms. The discharge current from the capacitor at 0^+ is $20 V / 3.75 k\Omega = 5.333$ mA and $20 V / 15 k\Omega = 1.333$ mA of it goes through the 10k in the direction marked at that instant. Therefore the zero-state response of this current for $I \delta(t)$ current excitation at input of the circuit = $1.333 e^{-2666.67 t}$ mA.

Time constant of a circuit containing single capacitor and multiple resistors can be determined by evaluating $R_{eq}C$ where R_{eq} is the equivalent resistance appearing across C after all independent sources have been deactivated.

Step Response of First-Order RC Circuits

Step Response is understood to be the zero-state response of the circuit when unit step input is applied to it. Hence the initial voltage across the capacitor is zero. It takes an impulse current flow through a capacitor to change its voltage by a non-zero finite amount instantaneously. Since there is no such impulse current flow in the present instance, the voltage across the capacitor remains zero at $t = 0^+$ too.

Consider the Series RC Circuit first. The applied voltage at $t = 0^+$ is 1 Volt and the voltage across the capacitor is constrained to remain at zero at that instant. And the circuit has to obey Kirchhoff's Voltage Law at that instant. This implies that the voltage across the resistor at that instant has to be 1 Volt and that a current of $1/R$ amps has to flow through the circuit at that instant. Since the rate of growth of a capacitor voltage is given by the charging current divided by capacitance value, the rate of change of $v_C(t)$ at $t = 0^+$ will be $1/RC$ Volts/sec. As the capacitor voltage grows, the voltage available across the resistor decreases; thereby bringing down the charging current in the circuit. Hence the capacitor keeps charging up with progressively decreasing rate. This is a typical first-order process. The capacitor voltage tends to reach 1 Volt as $t \rightarrow \infty$ and correspondingly the current through the circuit tends to go to zero.

'Impulse Response' is the short name for 'Zero-State Response with Unit Impulse Input'.

'Step Response' is the short name for 'Zero-State Response with Unit Step Input'.

6 Chapter 11 : RC and RLC Circuits in Time-Domain

The detailed solution may be worked out by either 'complementary solution plus particular integral' format or 'zero-input response plus zero-state response' format. But we can do better than that. We have already worked out the impulse response of the Series RC Circuit in this section. And we remember that for a lumped linear time-invariant circuit, the zero-state response gets integrated when the input source function gets integrated. Unit step function is the integral of Unit impulse function. Therefore step response must be the integral of impulse response.

Therefore,

$$\text{Impulse Response, } v_C(t) = \frac{1}{RC} e^{-t/\tau} \text{ volts for } t \geq 0^+, \text{ where } \tau = RC$$

$$\therefore \text{ Step Response, } v_C(t) = \int_0^t \frac{1}{RC} e^{-t'/\tau} dt' = (1 - e^{-t/\tau}) \text{ volts for } t \geq 0^+$$

$$\text{and } v_R(t) = 1 - v_C(t) = e^{-t/\tau} \text{ volts for } t \geq 0^+$$

$$i_R(t) = i_C(t) = \frac{v_R(t)}{R} = \frac{1}{R} e^{-t/\tau} \text{ amps for } t \geq 0^+$$

Now consider the Parallel RC Circuit excited by a unit step current source. The voltage across the capacitor at $t = 0^+$ remains at zero. Therefore all of the source current, i.e., 1 Amp has to flow through the capacitor. This results in charging up of capacitor with an initial charging rate of $1/C$ volts/sec. As the capacitor gets charged, the resistor takes its share of current and consequently the rate of rise of voltage comes down. Now we may write down the circuit solution straightaway - $v_C(t)$ must be a rising exponential tending towards R volts, $i_C(t)$ must be a decreasing exponential starting at 1 A and $i_R(t)$ must be a rising exponential moving to 1 A. All of them will have the same time constant of $\tau = RC$ sec.

$$\therefore \text{ Step Response, } v_C(t) = R(1 - e^{-t/\tau}) \text{ volts for } t \geq 0^+$$

$$i_C(t) = e^{-t/\tau} \text{ amps and } i_R(t) = (1 - e^{-t/\tau}) \text{ amps for } t \geq 0^+$$

These step response waveforms are plotted in Fig. 11.3-5.

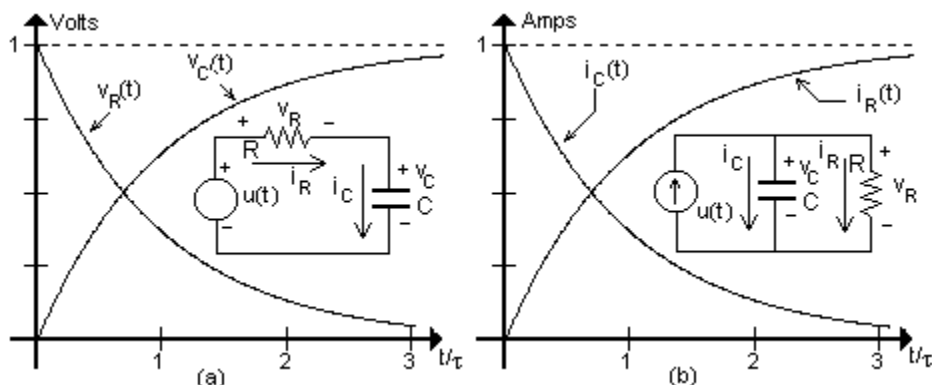


Fig. 11.3-5 Unit Step Response of RC Circuits (a) Series RC Circuit (b) Parallel RC Circuit

The zero-state responses in both cases contain a transient term (exponential in nature) and a steady-state response term (constant in nature). We had termed the steady-state response term as the *dc steady-state term* earlier. Since the current in a capacitor is proportional to the rate of change of its voltage, the only value of current such that both voltage and current in a capacitor remain constant in time is zero. It can have any constant voltage across it but its current is constrained to be zero under dc steady-state. Therefore, a capacitor may be replaced by an open-circuit for dc steady-state analysis.

The dc steady-state current in a Series RC Circuit is zero. This implies that there is energy flow from the dc source only during the charging process. After the capacitor has charged up fully there is no energy drain from the source. Consider the charging of a capacitor to V volts in a Series RC Circuit using a dc source of V volts.

If impulse response of a linear time-invariant circuit is known, its step response can be obtained by integrating its impulse response between the limits 0^+ and t .

This works since both impulse response and step response are zero-state responses. Note that only zero-state response gets integrated when input function gets integrated. Total response does not!

A capacitor may be replaced by an open-circuit for the analysis of dc steady-state response.

Many practical applications in Electrical and Electronics Engineering involve periodic charging and discharging of capacitors in systems operating from dc power supplies. The capacitors may be there by design or by way of parasitics.

$0.5CV^2$ Joules of energy is lost in the charging path every time a capacitor is charged to V volts from zero volts. $0.5CV^2$ Joules of energy is lost every time a capacitor charged to V volts is discharged to zero volts through a resistor or a passive path. Thus every charge-discharge cycle results in CV^2 Joules of energy loss. If f is the frequency of operation, the resultant power loss will be CV^2f watts.

This is a major factor that decides the heating in digital electronic gate circuits. This power loss along with the heat dissipation capability of the IC package place limitations on the frequency of operation of such devices. Especially so in the case of a family of digital electronic gates called CMOS devices. See Problem-10 at the end of this chapter.

$$\begin{aligned} \text{Total Energy Delivered by the Source} &= \int_{0^+}^{\infty} V \times \frac{V}{R} e^{-t/\tau} dt = CV^2 \text{ Joules} \\ \text{Total Dissipated by the Resistor} &= \int_{0^+}^{\infty} R [i_R(t)]^2 dt \text{ Joules} \\ &= \int_{0^+}^{\infty} R \left[\frac{V}{R} e^{-t/\tau} \right]^2 dt \text{ Joules} \\ &= \frac{CV^2}{2} \text{ Joules} \end{aligned}$$

Thus, the energy spent in charging up a capacitor to V volts is CV^2 Joules, half of which appears in the capacitor as electrostatic energy storage and the remaining half gets dissipated in the charging resistor. *This conclusion is independent of the value of resistance of the resistor.* However, we should not stretch it to the case where $R = 0!$ That is when all those *parasitic elements* that we neglected in modeling a real physical electrical device as a mathematical capacitance will start having their say in the matter.

Ramp Response of Series RC Circuit

Here too we employ the integration method to arrive at the zero-state response to unit ramp input from the zero-state response to unit step input since unit ramp waveform is the integral of unit step waveform.

$$\text{Ramp Response, } v_C(t) = \int_{0^+}^t (1 - e^{-t/\tau}) dt = t + \tau e^{-t/\tau} \Big|_{0^+}^t = t - \tau(1 - e^{-t/\tau}) \text{ volts for } t \geq 0^+$$

Ramp waveform finds application in many contexts in electronics, instrumentation and signal processing. It is used as the internal time-base waveform in oscilloscopes. It is used in timing and counting applications too. Some dedicated electronic circuitry generates this ramp waveform and the generated waveform is conducted to the application circuit by means of a two-wire connection. This two-wire connection can often be modeled approximately by a Series RC Circuit where the resistor is contributed by the output resistance of the generator circuit (*i.e.*, the resistor that appears in the Thevenin's equivalent of the generator circuit output) and the capacitor is contributed by the input capacitance of the application circuit. The ramp waveform gets modified in this process of transmission from the output of generator circuit to the input of the application circuit. We observe from the above expression for ramp response of Series RC Circuit that the ramp waveform suffers two modifications – in the initial portion, *i.e.*, for $t \ll \tau$, the output fails to follow the linear variation of input and is rather prominently an exponential waveform. For $t \gg \tau$ the output follows the input; but with a constant difference of τ volts. Hence, we may conclude that a Series RC Circuit will be able to transmit a ramp waveform more or less faithfully if the waveform duration is significantly larger than the time constant of the circuit. The waveforms in Fig. 11.3-6 show this clearly.

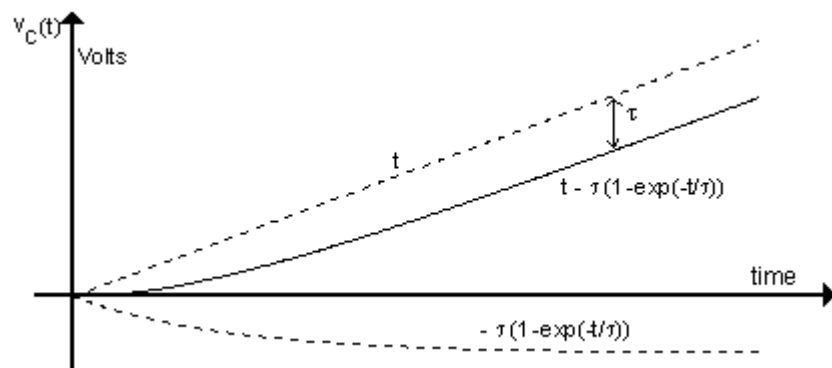


Fig. 11.3-6 Unit Ramp Response of Series RC Circuit

Series RC Circuit with Real Exponential Input

Consider a Series RC Circuit excited at the input by a real exponential voltage source of the form $v_s(t) = e^{-\sigma t} u(t)$ volts. The zero-state response under real exponential excitation in the case of a Series RL circuit was described in Section 10.9 in Chapter 10. The reader is referred to Eqn. 10.9-5 in Chapter 10. The zero-state response of capacitor voltage in the present case is written down by analogy from that equation as

$$v_C(t) = \left(\frac{\alpha}{\alpha - \sigma} \right) (e^{-\sigma t} - e^{-\alpha t}) \text{ volts for } t \geq 0^+ \text{ where } \alpha = 1/RC \text{ and } \alpha \neq \sigma. \quad (11.3-1)$$

This may also be expressed in terms of circuit time constant and excitation time constant as

$$v_C(t) = \left(\frac{1}{1 - \tau/\tau_e} \right) (e^{-(\tau/\tau_e)t_n} - e^{-t_n}) \text{ volts for } t \geq 0^+$$

where $\tau = RC, \tau_e = 1/\sigma, t_n = t/\sigma$ and $\tau \neq \tau_e$

The input source functions and corresponding capacitor voltage waveforms are shown in Fig. 11.3-7. Time is normalised to the base of circuit time constant in this figure.

The case with $\alpha = \sigma$ was avoided in Chapter 10 with a promise that it will be taken up later in a different context. We do not avoid it any longer. The case with $\alpha = \sigma$ is taken up now as a limiting case of Eqn. 11.3-1 as $\alpha \rightarrow \sigma$.

$$\begin{aligned} v_C(t) &= \left(\frac{\alpha}{\alpha - \sigma} \right) (e^{-\sigma t} - e^{-\alpha t}) \text{ for } t \geq 0^+ \\ &= \left(\frac{\alpha}{\alpha - \sigma} \right) \left[\left(1 - \sigma t + \frac{(\sigma t)^2}{2!} - \frac{(\sigma t)^3}{3!} + \frac{(\sigma t)^4}{4!} - \dots \right) \right. \\ &\quad \left. - \left(1 - \alpha t + \frac{(\alpha t)^2}{2!} - \frac{(\alpha t)^3}{3!} + \frac{(\alpha t)^4}{4!} - \dots \right) \right] \\ &= \left(\frac{\alpha}{\alpha - \sigma} \right) \left[(\alpha - \sigma)t - \frac{(\alpha^2 - \sigma^2)}{2!} t^2 + \frac{(\alpha^3 - \sigma^3)}{3!} t^3 - \frac{(\alpha^4 - \sigma^4)}{4!} t^4 + \dots \right] \\ &= (\alpha t) \left[1 + \sum_{i=2}^{\infty} (-1)^{i-1} \frac{(\alpha^i - \sigma^i)}{(\alpha - \sigma)i!} t^{i-1} \right] \\ (\alpha^i - \sigma^i) &= (\alpha - \sigma) \underbrace{(\alpha^{i-1} + \alpha^{i-2}\sigma + \alpha^{i-3}\sigma^2 + \dots + \alpha\sigma^{i-2} + \sigma^{i-1})}_{i \text{ terms}} \end{aligned}$$

$$\therefore \text{As } \alpha \rightarrow \sigma, \frac{(\alpha^i - \sigma^i)}{(\alpha - \sigma)} \rightarrow i \times \alpha^{i-1} \text{ and } v_C(t) \rightarrow (\alpha t) \left[1 + \sum_{i=2}^{\infty} (-1)^{i-1} \frac{i \times \alpha^{i-1}}{i!} t^{i-1} \right]$$

$$\text{i.e., } v_C(t) \rightarrow (\alpha t) \left[1 - \alpha t + \frac{(\alpha t)^2}{2!} - \frac{(\alpha t)^3}{3!} + \frac{(\alpha t)^4}{4!} - \dots \right]$$

$$\therefore v_C(t) = \alpha t e^{-\alpha t} = \left(\frac{t}{\tau} \right) e^{-\left(\frac{t}{\tau} \right)} \text{ volts for } t \geq 0^+$$

The waveshape of output voltage will be same as in Fig. 11.3-7. The output in this case will reach a maximum of $1/e = 0.3678$ volts at $t = \tau$ sec.

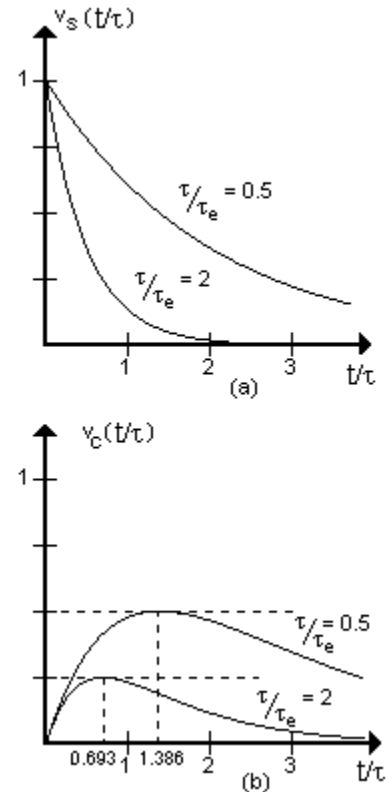


Fig. 11.3-7 Zero-State Response of RC Circuit for Exponential Input (a) Input Wave (b) Capacitor Voltage

Example : 11.3-2

Two first-order Series RC Circuits are cascaded using a unity gain buffer amplifier as shown in Fig. 11.3-8. Find the output $v_o(t)$ as a function of time if the circuit is initially relaxed.

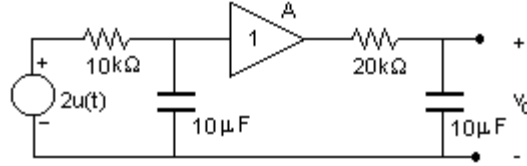


Fig. 11.3-8 Circuit for Example : 11.3-2

Solution

The unity gain buffer amplifier in between prevents any loading-interaction between the two RC circuits. This implies that the response of the first RC stage is independent of the presence of the second stage. The first stage produces a voltage across its capacitor that is accepted by second stage as its input source function as if it is coming from an ideal independent voltage source.

Let $v_1(t)$ be the response voltage at the terminals of the first capacitor. Then $v_1(t)$ is twice the zero-state response to unit step input (*i.e.*, step response).

The time constant of first stage is $10\text{k}\Omega \times 10\mu\text{F} = 100\text{ms} = 0.1 \text{ s}$.

$$\therefore v_1(t) = 2(1 - e^{-10t}) \text{ volts for } t \geq 0^+$$

This voltage is the input to second stage since the gain of the buffer amplifier is unity. This input may be treated as sum of two inputs $-2u(t)$ and $-2e^{-10t}u(t)$.

Zero-state response of a lumped linear time-invariant circuit obeys superposition principle and hence the responses to these inputs may be found out individually and be superposed to get the desired response.

The time constant of second stage is $20\text{k}\Omega \times 10\mu\text{F} = 200\text{ms} = 0.2 \text{ s}$.

The component contributed to $v_o(t)$ by $2u(t)$ is $2(1 - e^{-5t})$ volts.

The contribution to $v_o(t)$ by $-2e^{-10t}u(t)$ is obtained by using Eqn. 11.3-1 with $\alpha = 5$ and $\sigma = 10$. This contribution is $-2 \times -(e^{-10t} - e^{-5t})$ volts for $t \geq 0^+$.

Therefore ,

$$\begin{aligned} v_o(t) &= 2(1 - e^{-5t}) + 2(e^{-10t} - e^{-5t}) \text{ volts for } t \geq 0^+ \\ &= 2 - 4e^{-5t} + 2e^{-10t} \text{ volts for } t \geq 0^+ \end{aligned}$$

The variation of capacitor voltages $v_1(t)$ and $v_2(t)$ as functions of time is shown in Fig. 11.3-9.

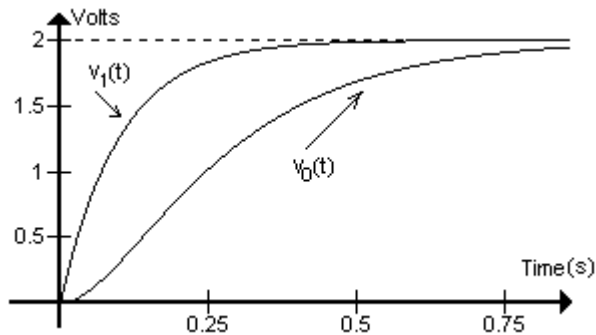


Fig. 11.3-9 Output Waveforms Across RC Stage Capacitors in Example : 11.3-2

Example : 11.3-3

Two first-order Series RC Circuits are cascaded non-interactively by employing a unity gain buffer amplifier as shown in Fig. 11.3-10. The voltage across the resistor of the first RC stage is the input to the second stage and the voltage across the capacitor of the second stage is the desired output. Find the step response of the system.

Solution

Let $v_1(t)$ be the voltage across the $10k\Omega$ resistor in the first stage. We know that the zero-state step response of capacitor voltage in a Series RC Circuit is $(1-e^{-t/\tau})$ where τ is the time constant of the circuit given by RC product. The voltage across capacitor and the voltage across resistor will have to add up to 1 Volt for all $t \geq 0^+$ in step response of a Series RC Circuit. Therefore the step response of voltage across the $10k\Omega$ resistor is $[1-(1-e^{-t/\tau})] = e^{-t/\tau}$ volts. The time constant of the first stage is 0.1 s.

$$\therefore v_1(t) = e^{-10t} \text{ volts for } t \geq 0^+$$

This voltage is the input to the second stage. Its time constant is 0.01 s. We use Eqn. 11.3-1 to obtain $v_o(t)$ with $\alpha = 100$ and $\sigma = 10$.

$$\therefore v_o(t) = \left(\frac{100}{100-10} \right) (e^{-10t} - e^{-100t}) = 1.111 (e^{-10t} - e^{-100t}) \text{ volts for } t \geq 0^+$$

Note that the steady-state value of step response is zero. This is so because the first capacitor effectively opens the circuit for dc under steady-state. All the dc content of source voltage will be found across the first capacitor in the steady-state.

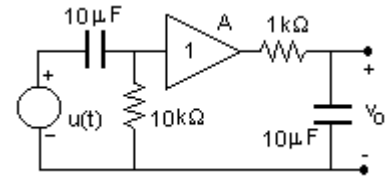


Fig. 11.3-10 Circuit for Example : 11.3-3

Example : 11.3-4

Show that the two circuits shown in (a) and (b) of Fig. 11.3-11 have the same step response except for a sign change. The operational amplifier may be treated as an ideal one. Compare the currents drawn from the voltage source by the circuits.

Solution

The time constant of the circuit in (a) of Fig. 11.3-11 is 100ms = 0.1 s and its step response is $(1-e^{-10t})$ volts for $t \geq 0^+$.

Consider the circuit in (b) of Fig. 11.3-11. The Opamp is connected with negative feedback. Further, we assume that the input voltage applied is of such magnitude that the Opamp does not enter voltage saturation at its output. Moreover, we assume that the Opamp has sufficiently large slew rate capability such that it never enters rate limited operation. With these assumptions, we can analyse the Opamp using its ideal model.

The non-inverting terminal of Opamp is grounded and by *virtual short* principle the inverting input terminal is also *virtually grounded*. Therefore, the current that flows through R_1 is $u(t)/R_1$. Since the current into the input terminals of an ideal Opamp is zero, this current flows into the R_2/C combination connected in the feedback path of the Opamp. The voltage developed across this parallel combination is nothing but a scaled version of step response of a Parallel RC Circuit with step current excitation. The scaling factor is $1/R_1$. This step response is $R_2(1-e^{-10t})$ since the time constant involved is 0.1 s. Therefore, the voltage developed across the parallel combination in the feedback path is $(R_2/R_1) (1-e^{-10t})$ volts with its positive polarity at the inverting input of Operational amplifier. Since the inverting input is at *virtual ground*, the voltage of output terminal with respect to ground (reference point) is the negative of this voltage (by KVL).

$$\therefore v_o(t) = -\frac{R_2}{R_1} (1-e^{-10t}) = -(1-e^{-10t}) \text{ volts for } t \geq 0^+ \text{ since } R_1 = R_2 = 10k\Omega$$

Therefore the two circuits in Fig. 11.3-11 have the same step response (and hence same dynamic behaviour) except for a change in sign.

The voltage across R in the circuit (a) is $[1-(1-e^{-10t})] = e^{-10t}$ volts and therefore the current drawn from the unit step voltage source by this circuit is $0.1 e^{-10t}$ mA for $t \geq 0^+$. But the current drawn by the second circuit is $u(t)/R_1 = 0.1$ mA for $t \geq 0^+$. Thus, the

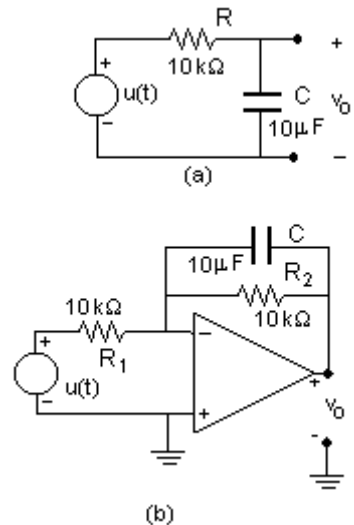


Fig. 11.3-11 Circuits for Example : 11.3-4

second circuit presents a constant input resistance level to the applied voltage source whereas the first circuit presents a time-varying input resistance level to the source. If the voltage source is not an ideal one, *i.e.*, if it has a non-zero internal resistance, the time constant of circuit in (a) will change and hence the shape of its step response will change. However, the shape of step response will not change in the case of circuit (b); but the initial magnitude will change due to change in the ratio (R_2/R_1) .

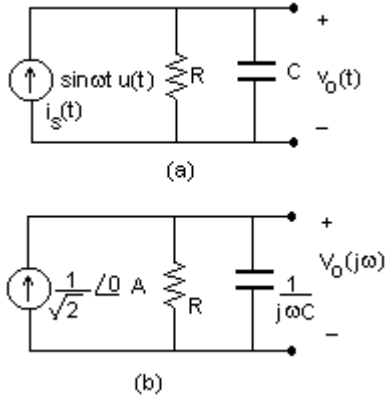


Fig. 11.3-12 (a) Parallel RC Circuit with Sinusoidal Excitation and (b) its Phasor Equivalent

Zero-State Response of Parallel RC Circuit for Sinusoidal Input

The zero-state response for sinusoidal input for any linear time-invariant circuit can be obtained in three ways.

- 1) Let the input be $\sin(\omega t) u(t)$. Obtain the zero-state response of the circuit for a complex exponential input function e^{st} where s is a complex number. Substitute $s = j\omega$ in the solution and accept the *imaginary part of the solution* as the zero-state response for $\sin(\omega t) u(t)$.
- 2) Express $\sin(\omega t)$ as $[(e^{j\omega t} - e^{-j\omega t})/2j]$ by using Euler's formula, get the zero-state responses for the two exponential functions separately and use superposition principle.
- 3) Use phasor method to obtain the sinusoidal steady-state response and add a transient response term such that the total response satisfies initial conditions. Initial conditions will be zero-valued since we are dealing with zero-state response.

The first two methods were already illustrated in the context of sinusoidal response of RL circuits in Chapter 10. We use the third method here to obtain the zero-state response for the voltage appearing across a Parallel RC Circuit excited by a sinusoidal current source with source function of $\sin(\omega t) u(t)$ amps.

The circuit in time-domain and phasor-domain are shown in (a) and (b) of Fig. 11.3-12 respectively.

$$\begin{aligned} V_o(j\omega) &= R // \left(\frac{1}{j\omega C} \right) \times \frac{1}{\sqrt{2}} \angle 0 = \frac{R}{1 + j\omega RC} \times \frac{1}{\sqrt{2}} \angle 0 = \frac{R}{1 + jk} \times \frac{1}{\sqrt{2}} \angle 0; k = \omega RC = \omega\tau \\ &= \frac{R}{\sqrt{1+k^2}} \angle -\phi \times \frac{1}{\sqrt{2}} \angle 0; \phi = \tan^{-1} k \end{aligned}$$

Going back to time-domain, we get the steady-state component of voltage across the Parallel RC Circuit as

$$\frac{R}{\sqrt{1+k^2}} \sin(\omega t - \tan^{-1} k) \text{ with } k = \omega\tau.$$

Now we add a transient component of known form $Ae^{-t/\tau}$ and evaluate A such that the total solution is zero at $t = 0^+$. We get,

$$A = \frac{R}{\sqrt{1+k^2}} \sin(\tan^{-1} k)$$

$$\text{Since } \tan^{-1} k \text{ lies in first quadrant, } \sin(\tan^{-1} k) = \frac{k}{\sqrt{1+k^2}}$$

$$\therefore A = \frac{R}{\sqrt{1+k^2}} \frac{k}{\sqrt{1+k^2}} \text{ and}$$

$$v_o(t) = \frac{R}{\sqrt{1+k^2}} \left(\sin(\omega t - \tan^{-1} k) + \frac{k}{\sqrt{1+k^2}} e^{-t/\tau} \right) \text{ for } t \geq 0^+$$

We normalise the time variable using the circuit time constant as the base and the output voltage by using the value of R as the base value and obtain the following expression for normalised voltage $v_{on}(t)$ as a function of normalised time t_n .

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$$v_{on}(t) = \frac{1}{\sqrt{1+k^2}} \left(\sin(kt_n - \tan^{-1} k) + \frac{k}{\sqrt{1+k^2}} e^{-t_n} \right) \text{ for } t_n \geq 0^+ \quad (11.3-2)$$

where $v_{on}(t) = \frac{v_o(t)}{R}$ and $t_n = \frac{t}{\tau}$

This waveform for a case with $k = 4$ is shown in Fig. 11.3-13.

Normalised voltage across a Parallel RC circuit excited by a sinusoidal current source

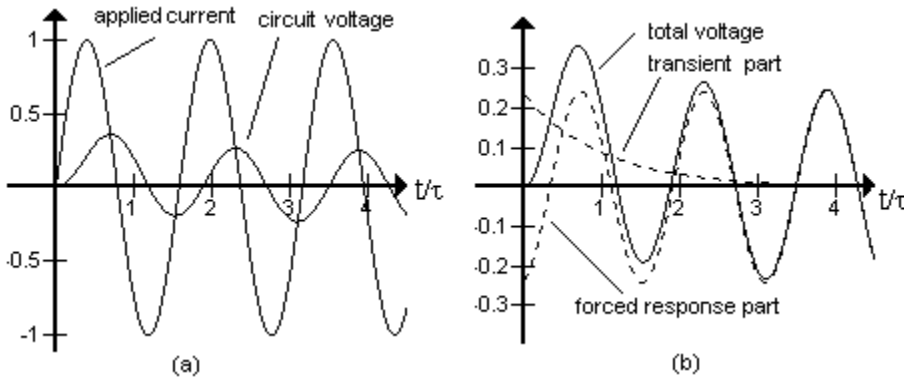


Fig. 11.3-13 Unit Sinusoidal Response (Normalised) of a Parallel RC Circuit with $k = 4$

We had noted under a similar context (Section 10.9 in Chapter 10 on RL Circuits) that the number k can be interpreted as a comparison between the characteristic time, *i.e.*, the period of the applied input and the characteristic time of the circuit, *i.e.*, its time constant. k can be expressed as $2\pi(\tau/T)$ where T is the period of input. The value of T is indicative of the rate of change involved in the waveform, *i.e.*, the *speed* of the waveform. Time-constant is a measure of inertia in the system. Therefore, an input sinusoid is too fast for a circuit to follow if its T is smaller than the time constant τ of the circuit. Similarly, if input sinusoid has a T value much larger than time constant of the circuit, the circuit will perceive it as a very slow waveform and will respond almost the same way it does to dc input. These aspects are clearly brought out in the expression in Eqn. 11.3-2.

We make the following observations on the sinusoidal steady-state response of Parallel RC Circuit with *current source excitation* from Eqn. 11.3-2.

- The circuit voltage under sinusoidal steady-state response is a sinusoid at the same angular frequency ω rad/sec as that of input current sinusoid.
- The circuit voltage initially is a mixture of an exponentially decaying unidirectional transient component along with the steady-state sinusoidal component. This unidirectional transient imparts an offset to the voltage during the initial period.
- The circuit voltage at its first peak can go close to twice its steady-state amplitude in the case of circuits with $\omega\tau \gg 1$ due to this offset.
- The amplitude of sinusoidal steady-state response is always less than corresponding amplitude when a dc input is applied. This is due to the capacitive inertia of the circuit. When input is a current, capacitance in a circuit behaves as electrical inertia, and, when input is a voltage, inductance in a circuit behaves as electrical inertia. The amplitude depends on the product $\omega\tau$ and decreases monotonically with the $\omega\tau$ product for fixed input amplitude.
- The response sinusoid (voltage) lags behind the input sinusoid (current) under steady-state conditions by a phase angle that increases monotonically with $\omega\tau$.
- The frequency at which the circuit gain becomes $1/\sqrt{2}$ times that of dc gain is termed as a *cut-off frequency* and since this takes place as we go up in frequency it is called *upper cut-off frequency*. Upper cut-off frequency of Parallel RC Circuit is at $\omega = 1/\tau$ rad/sec. The phase at this frequency will be -45 degrees.
- Circuit voltage amplitude becomes very small at high frequencies ($\omega\tau \gg 1$) and the voltage lags the input current by $\approx 90^\circ$ at such frequencies.

Time-constant of a circuit is a measure of inertia in the circuit.

If the typical time of variation of input is small compared to the time constant of the circuit the circuit perceives the input as a fast one and the response will be small-valued.

If the time of variation of input is large compared to time constant, the circuit perceives such input as a slow one and responds almost the same way as it responds to dc input.

Definition of Upper Cut-off Frequency

11.4 Periodic Steady-State in a Series RC Circuit

When a *repetitive input* is applied to a linear time-invariant circuit, the output is a mixture of the circuit natural response terms and forced response terms during the initial few cycles of operation.

However, after a few cycles, the circuit settles down to a mode of operation in which the output starts with a value at the beginning of the cycle and returns to the same value at the end of that cycle only to repeat that process again in the next cycle.

When the circuit reaches this kind of *repetitive* operation under the influence of any *repetitive* input, it is said to have reached a *periodic steady-state* with respect to that input.

Sinusoidal steady-state is a special case of periodic steady-state.

We address the issue of zero-state response to *repetitive input* in RC circuits in this section and consider a specific example for doing so. Refer to Fig. 11.4-1.

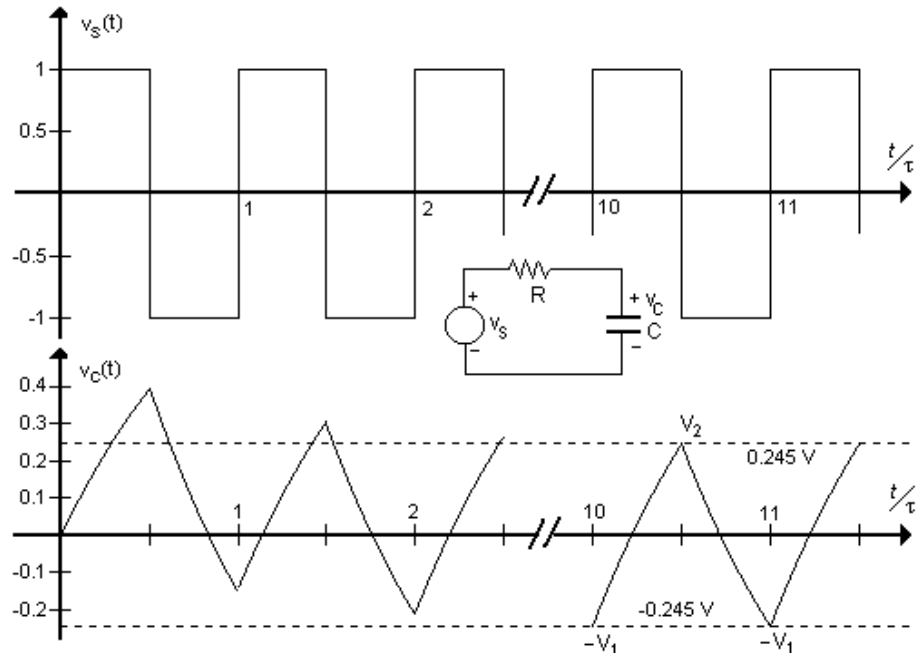


Fig. 11.4-1 Series RC Circuit with Repetitive Square Wave Input

A symmetric square wave voltage with 1 V amplitude is applied from $t = 0$ to an initially relaxed Series RC Circuit. The period of the square wave is assumed to be equal to the time constant and the time scale is marked in terms of t/τ .

A step response starts at $t = 0$ and takes the output to $(1 - e^{-0.5}) = 0.3935$ V at $t/\tau = 0.5$. Another zero-state step response starts in the negative direction at that point along with a zero-input response corresponding to an initial voltage of 0.3935 V on the capacitor. Thus the output waveform can be expressed as $= 0.3935 e^{-(t-0.5\tau)/\tau} - (1 - e^{-(t-0.5\tau)/\tau})$ for the time range $0.5 \leq t/\tau \leq 1$. This expression may be evaluated at $t/\tau = 1$ to get the initial condition at that point and a new expression valid for $1 \leq t/\tau \leq 1.5$ may be obtained as a superposition of zero-input response and a new zero-state step response. This way the solution may be taken forward.

It may be observed that the values of capacitor voltage at the beginning and at the end of a cycle are not the same in the first few cycles of operation. However, after a few cycles, the circuit settles down to a mode of operation in which the output starts out with a particular value at the beginning of the cycle and returns to the same value at the end of that cycle only to repeat that process again in the next cycle. This means that the output too reaches a *repetitive* pattern after a few initial cycles. When the circuit reaches this kind of *repetitive* operation under the influence of any *repetitive* input, it is said to have reached a *periodic steady-state* with respect to that input. Fig. 11.4-1 shows that the capacitor voltage oscillates between 0.245 V and -0.245 V under periodic steady-state in the present instance where T – the period of input – has been taken to be equal to τ , the time constant of the circuit.

It is not necessary to start at the beginning and march forward till the circuit reaches the periodic steady-state in order to find out the amplitude under steady-state condition. We can proceed in the following manner to develop an expression for this amplitude.

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Let $-V_1$ and $+V_2$ be the negative and positive amplitudes in a cycle as shown in Fig. 11.4-1. Then the circuit would have reached steady-state when the output value at the end of the cycle turns out to be exactly $-V_1$.

$$v_C(t) = -V_1 e^{-t/\tau} + \left(1 - e^{-t/\tau}\right) \text{ for } 0 \leq t \leq T/2 \text{ with } t \text{ measured}$$

from the beginning of cycle after the circuit has reached periodic steady - state

$$\therefore V_2 = -V_1 e^{-0.5T/\tau} + \left(1 - e^{-0.5T/\tau}\right)$$

$$v_C(t) = V_2 e^{-(t-0.5T)/\tau} - \left(1 - e^{-(t-0.5T)/\tau}\right) \text{ for } T/2 \leq t \leq T$$

This expression evaluated with $t=T$ should be equal to $-V_1$ under periodic steady - state.

$$\therefore -V_1 = V_2 e^{-0.5T/\tau} - \left(1 - e^{-0.5T/\tau}\right)$$

Substituting for V_2 in terms of V_1 and solving for V_1 , we get ,

$$V_1 = \frac{1 - e^{-T/2\tau}}{1 + e^{-T/2\tau}} \text{ and } V_1 = V_2$$

This expression evaluated with $T/\tau = 1$ gives $V_1 = V_2 = 0.245$ V for a 1 V amplitude square wave input.

The key to the above derivation was our knowledge of step response of Series RC Circuit. The input could be thought of as a sequence of unit steps and hence the output could be strung together employing step response and zero-input response segments. Square waves and more generalised versions of it (the so-called *rectangular pulse waveforms* that are 'suarish' waveforms with unequal half-cycle duration and unequal positive and negative amplitudes) appear very frequently in Pulse Electronics Applications and Digital Electronics. And, Series RC Circuits are routinely used to model the transmission channel that takes such signals from one location to another location in the electronic system. Hence periodic steady-state of Series RC Circuit under rectangular pulse waveforms is of crucial significance in Analog and Digital Electronics. This is the motivation behind this section on periodic steady-state.

The method described above for finding out steady-state amplitudes under repetitive excitation will work only if we can identify the repetitive waveform as a sequence of some well-known shape like a step or ramp or sinusoid. However, in practice, we will be called upon to solve for periodic steady-state even when the period of input is of a complex shape. How do we proceed? The answer lies in *frequency response* of the circuit.

11.5 Sinusoidal Steady-State Frequency Response of First Order RC Circuits

The concept of *sinusoidal steady-state frequency response* was already introduced in Chapter 10 in the context of RL Circuits. Essentially, we apply a sinusoidal input of suitable amplitude to a circuit and wait for enough time for the transient response to die down. After steady-state is satisfactorily established in the circuit, we measure the amplitude of output and its phase with respect to the input sine wave. We repeat this process for various values of frequency of input. We ensure that the circuit is in steady-state before we measure the output every time. The data so obtained is plotted to show the variation of ratio of output amplitude to input amplitude and phase of steady-state voltage against $k (= \omega\tau)$. Such a pair of plots will constitute what is called the *ac steady-state frequency response plots* for this circuit. The ratio of output amplitude to input amplitude is called the *gain* of the circuit. Its dimension will depend on the nature of input and output quantities.

The same data can be obtained from the analytical model of the circuit if such a model exists. Consider the Series RC Circuit and its phasor model shown in Fig. 11.5-1.

If one period of the repetitive input is piece-wise linear, it is possible to calculate the periodic steady-state by employing the method illustrated here for a square wave input.

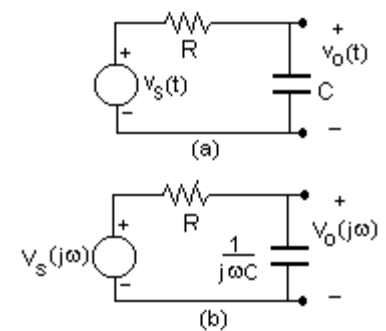


Fig. 11.5-1 Series RC Circuit and its Phasor Model

Frequency Response Function ,

$$H(j\omega) = \frac{V_o(j\omega)}{V_s(j\omega)} = \frac{1/j\omega C}{R + 1/j\omega C} = \frac{1}{1 + j\omega RC} \tag{11.5-1}$$

$$= \frac{1}{1 + j\omega\tau} = \frac{1}{\sqrt{1 + (\omega\tau)^2}} \angle -\tan^{-1}(\omega\tau)$$

The Gain and Phase plots for the circuit are shown in Fig. 11.5-2. The gain goes to 70.7% level at $\omega = 1/\tau$ rad/sec and phase delay at that frequency is 45° .

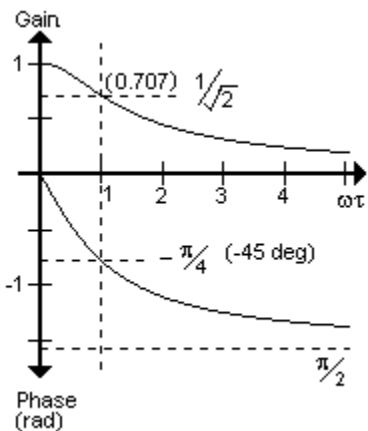


Fig. 11.5-2 Frequency Response Plots for Series RC Circuit

The Use of Frequency Response

Frequency Response information helps us to find the *steady-state output* when the input is a *mixture of sinusoids of different frequencies*. A sinusoid with a particular angular frequency is a periodic waveform. But a sum of many sinusoids with arbitrary frequencies need not be periodic. A special case where the sum of many sinusoids results in a periodic waveform is the one in which the sinusoidal components are of frequencies which are related *harmonically* - i.e., when all the frequencies are integer multiples of some basic frequency value. This is an important practical case.

Before we proceed to employ frequency response to solve circuits excited by sum of sinusoids, let us settle an issue regarding superposition principle. We know that zero-state responses due to multiple sources acting simultaneously can be obtained by superposition. But does it work for steady-state response component too?

Zero-state response contains two components – the transient response part and the steady-state response part. The transient response components, whether from zero-state response or zero-input response, will vanish with time if the circuit is passive and stable. Therefore superposition principle can be applied on steady-state response components.

Now, if the input contains many sinusoids with different frequencies, the steady-state response component due to each sinusoid may be obtained from frequency response plots and these components may be added up to obtain the complete steady-state response. This procedure is illustrated in the case of a Series RC Circuit with a time constant of 1 sec and with an input of $v_s(t) = (\sin t + 0.33 \sin 3t + 0.2 \sin 5t) u(t)$ volts. The output is taken across the capacitor.

Consider the first sinusoid that has an angular frequency of 1 rad/sec. The gain of the circuit at this frequency is 0.707 and phase delay is 45° (0.79 rad) (either from Eqn. 11.5-1 or from Fig. 11.5-2 with $\tau = 1$ s). Therefore, the steady-state component due to this sinusoid is $0.707 \sin(t - 0.79)$ volts. The second sinusoid of $0.33 \sin 3t$ with an angular frequency of 3 rad/sec meets with a gain of 0.3162 and phase delay of 71.57° (1.25 rad). Therefore, the steady-state component due to this sinusoid is $0.104 \sin(3t - 1.25)$ volts. Similarly, the third sinusoid of $0.2 \sin 5t$ with an angular frequency of 5 rad/sec meets with a gain of 0.1961 and phase delay of 78.7° (1.37 rad). Therefore, the steady-state component due to this sinusoid is $0.04 \sin(5t - 1.37)$ volts. $\therefore v_o(t) = 0.707 \sin(t - 0.79) + 0.104 \sin(3t - 1.25) + 0.04 \sin(5t - 1.37)$ volts. The input and output waveforms are shown in Fig. 11.5-3.

Steady-state response of a linear time-invariant circuit for a mixture of sinusoidal inputs at different frequencies can be obtained by applying superposition principle.

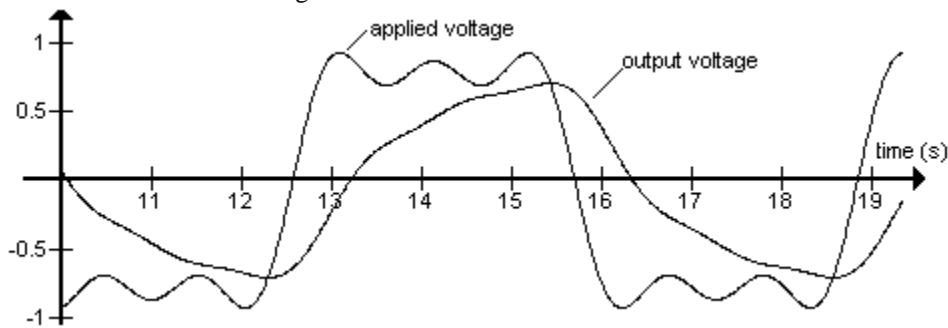


Fig. 11.5-3 Steady-State Response of Series RC Circuit for Mixed Sinusoidal Input

Frequency Response and Linear Distortion

We observe that our Series RC Circuit has meted out differential treatment to various sinusoids in the input mixture. It has shown a clear preference to the sinusoid with lowest frequency (with 1 rad/sec) and passed it on with only about 30% loss of amplitude whereas the remaining two sinusoids with 3 rad/sec and 5 rad/sec frequencies suffered 68.5% and 80% loss of amplitude respectively. Circuits that preferentially pass low frequency sinusoids to the output and curtail high frequency sinusoids are called *low-pass filters*. Low-pass filters will have a frequency response with a gain function that tapers down to zero as frequency goes up. Thus a Series RC Circuit with output taken across the capacitor is a first order low-pass filter. It shows a tendency to remove high frequency components in the input.

Further, we observe from Fig. 11.5-3 that the waveshape of output voltage is considerably different from that of input. This is inevitable in a filtering context. After all, some frequency components get removed or attenuated considerably in a filtering process and therefore the output can not but look different compared to input! When the waveshape of output under steady-state in a circuit is different from the waveshape of input, the circuit is said to have *distorted* the signal. Thus, *distortion* invariably follows *filtering*. When the change in waveshape is the desired outcome we call it *filtering*; when the change in waveshape is the undesired outcome we call it *distortion*.

This distortion of waveshape arises out of two reasons. Sinusoids at different frequencies meet with different gains in the circuit and therefore the mix of amplitudes, *i.e.*, the relative ratio of amplitudes of various sinusoids, will be different at output and input. In the example we considered, the ratio was 1:0.33:0.2 at input and 1:0.147:0.057 at the output. Waveshape changes due to this change in amplitude mix. Distortion arising out of this mechanism is called *amplitude distortion* and it is due to the gain response part of frequency response.

The second cause of distortion comes from phase response. Each sinusoid suffers a time delay when it goes through the circuit – the time delay is measured between zero crossing of that sinusoid in the input and in the output. Phase delay is equal to time delay multiplied by angular frequency. Thus the 1 rad/sec component in the previous example underwent a delay of 0.79 sec , the 3 rad/sec component suffered a delay of 1.25 rad/ 3 rad/sec = 0.42 sec and the 5 rad/sec component was subjected to a delay of 1.79 rad/5 rad/sec = 0.36 sec.

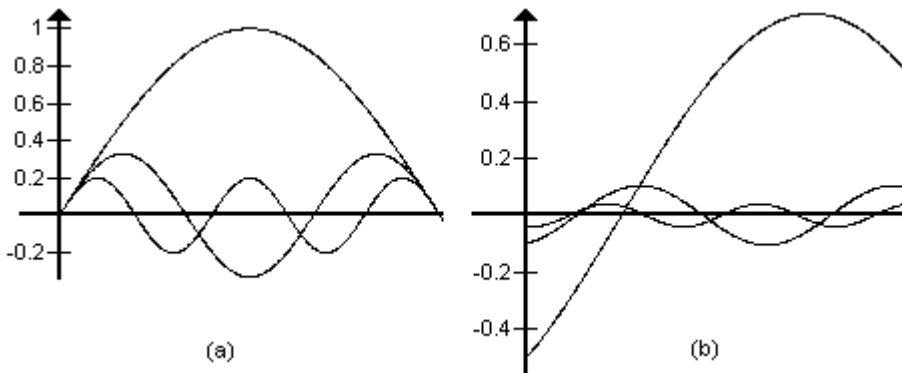


Fig. 11.5-4 Illustrating Phase Distortion Due to Dispersion

All the three cross the time-axis simultaneously at the input. But at the output they do not cross the time-axis simultaneously – the 5 rad/sec crosses first followed by the 3 rad/sec component and the 1 rad/sec component is the last one to cross time-axis. Thus, they get *dispersed*. This *dispersion* results in change in waveshape. Refer to Fig. 11.5-4. The three components in the input are shown in (a) and the corresponding components in the output are shown in (b). The dispersion in zero-crossing instants is clearly brought out in (b). The distortion resulting from dispersion of components brought about by *unequal time delays* suffered by the components in going through the circuit is termed as *phase distortion*. Of course, in any distortion context these two – amplitude distortion and phase distortion – are mixed up and can not be separated out.

Dynamic circuits provide differential treatment to various sinusoids when input is a mixture of sinusoids at different frequencies.

Such differential treatment makes the output waveshape different from input waveshape.

Such a change in the waveshape is called *distortion* or *filtering* depending upon the application context.

Amplitude distortion due to frequency response

Phase distortion from waveform dispersion due to unequal phase delays in frequency response

Phase distortion arises essentially due to phase response part of frequency response. If all the sinusoids are delayed by *same time delay* there will be no change in waveshape (assuming there is no amplitude distortion). The entire input waveshape will get bodily shifted in time-axis by a definite delay and will appear as output in that case. Therefore, either zero time delay for all frequencies or constant time delay for all frequencies will prevent phase distortion. A constant time delay implies that the phase delay must be a *linear function of ω* .

Conditions for no waveform distortion

The conditions to be satisfied by a circuit such that there is no waveshape distortion when a signal passes through it must be evident now – *its frequency response must have a gain that is flat with ω and a phase which is either zero or linear on ω , i.e., of the form $\phi = -k\omega$ where k is a real number*. Obviously only a memory-less circuit can satisfy this. Hence a circuit which contains at least one inductor or capacitor will cause waveshape distortion in general. Similarly, we conclude that a memory-less circuit can not function as a *filter*; we will need inductors and capacitors for that.

We observe that, in the example we analysed in this section, the input contained three sinusoids of 1 rad/sec, 3 rad/sec and 5 rad/sec and the output contained exactly three sinusoidal components with the same frequencies as in the input. In short, the circuit did not change the frequency of sinusoids. Neither did it generate a sinusoid with a frequency that was not there in the input. This, in fact, is a property of any lumped linear time-invariant (LLTI) system. They can only scale, differentiate or integrate signals. And these three mathematical operations can not produce a sinusoid with a frequency that is different from that of input. *Therefore a single frequency sinusoid can not suffer waveshape distortion in passing through a linear time-invariant circuit.*

Linear distortion versus non-linear distortion in Circuits

However, a non-linear circuit can change the waveshape of a single frequency sinusoid. Apply about 10mV of 1kHz sinusoidal voltage to a 741 Operational Amplifier non-inverting pin after grounding the inverting pin. The Operational Amplifier is in the open loop and its large gain results in output getting saturated. We will observe a waveform that is almost a square wave at the output. That is *non-linear distortion*. The waveshape distortion we observed in the example in this section was not due to non-linearity. It occurred due to differential treatment experienced by various sinusoidal components in a mixture of sinusoids when they went through the circuit. The distortion which occurs due to frequency response of a linear circuit is termed as *linear distortion* in order to distinguish this kind of distortion from distortion due to non-linearity. *Amplitude Distortion* and *Phase Distortion* are the two inseparable components of *Linear Distortion*.

Different filtering functions may be available from the same circuit

One should not be under the impression that the Series RC Circuit can function only as a low-pass filter. In fact, the kind of filter realised by a given circuit will strongly depend on where exactly is the input applied and where exactly is the output taken. A Series RC Circuit excited by a voltage source at the input of the series combination with output taken across the capacitor is a low-pass filter. The same circuit with same excitation but with output taken across the resistor is a high-pass filter that passes the high frequency sinusoids to the output and curtails the low frequency components including dc.

Jean Baptiste Joseph Fourier and Frequency Response

We look ahead a bit in this sub-section.

We used $v_s(t) = (\sin t + 0.33 \sin 3t + 0.2 \sin 5t) u(t)$ as an input to a Series RC Circuit in the previous sub-sections which dealt with the use of frequency response to solve for steady-state response when input is a mixture of sinusoids of different frequencies. We observe from Fig. 11.5-3 that $v_s(t)$ is a periodic wave. This is so because all the three sinusoids involved are periodic with a period of 2π sec. True, the sinusoid with 3 rad/sec frequency is periodic with a period of $2\pi/3$ sec. But if it is periodic with a period of $2\pi/3$ sec, it is periodic with a period of 2π sec too since there will be three full cycles of it in that duration. Therefore, in general, sum of sinusoids with frequencies which are integer multiples of some basic frequency (called fundamental frequency) will be a periodic waveform with period corresponding to the fundamental frequency.